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Single-phase boost DC-link integrated cascaded multilevel inverter for PV applications

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Abstract: This study presents a new boost DC-link integrated multilevel inverter (BDIMLI) topology for single-phase stand-alone photovoltaic applications. The BDIMLI is realised by the integration of two two-level boost DC-link converters (TBDCs) with a hybrid H-bridge inverter using symmetrical voltage sources. Conventional cascaded multilevel inverters require a large number of isolated DC source and circuit components. On the other side, switched capacitor multilevel inverter topologies require less number of sources and components, but need bulky capacitors. The proposed TBDC units charge the capacitors to the desired voltage with the high switching frequency, hence require less capacitance and component count. The proposed topology with proper selection of capacitor voltage levels can produce 9-, 11- and 13-level outputs without altering any circuit components. Besides, the proposed topology produces low-frequency common-mode voltage. The comprehensive analysis of BDIMLI in comparison with recent multilevel inverter topologies is presented. An experimental prototype of BDIMLI is built and its dynamic behaviour with different load conditions is presented for both 9- and 13-level operations.

1 Introduction

Application of multilevel inverter (MLI) is magnified in each domain of electrical engineering like renewable energy grid-tie systems, electric vehicles, electric drives etc. Compared to conventional two-level inverters, MLIs provide a high-quality output voltage, reduced dv/dt, low switching frequency, less filter size and reduced common-mode voltage (CMV) [1].

In general, MLI topologies are classified as neutral-point-clamped MLI (NPCMLI) [2], flying capacitors MLI (FCMLI) [3] and cascaded H-bridge MLI (CHBMLI) [4, 5]. Due to notable performance, these MLIs are adopted by electric drives and power quality related industries. NPCMLI and FCMLI topologies require a high component count (diodes, capacitors and it's rectification circuitry to address voltage unbalance), while CHBMLIs need multiple isolated voltage sources. Thus, it leads to increased cost and reduced efficiency. A few MLI topologies are reported with reduced switch count and voltage sources [6–11] to improve compactness and efficiency. New pulse-width modulation (PWM) techniques [9] are presented to maintain constant CMV and reduce leakage currents in cascaded half-bridge MLI topologies. Also, fault-tolerant methods [10] are incorporated for reduced switch count SCMLI (RSCMLI). However, none of these topologies offers high gain boost factor, which is essential in renewable energy applications.

In recent times, several boost derived MLIs are reported using boost converter [12], Z-source network [13, 14], coupled inductor [15] and switched capacitor (SC) [16–18] techniques. Z-source network and coupled inductor-based step-up MLIs provide high voltage gains owing to high switching stress and losses, while SCMLI topologies provide high efficiencies but require large capacitor size and switch count. SC cell comprised CHBMLI [16] with low capacitor size is proposed for high-frequency applications. Further, similar structures with large capacitor size for power frequency applications are adopted. The SCMLI topologies presented in [16] use parallel charging and series discharging of the capacitor. Hence the size of the capacitor is a function of frequency and load resistance. Modified H-bridge based SCMLI topologies similar to [9] are reported to further reduce the switch count. These SCMLI topologies provide high modularity and reliability, but the absence of the charging path and elongated discharging time intervals may lead to adverse drooping of capacitor voltage. Thus, a large capacitor is required to limit the ripple voltage, also, the increase in the capacitor size results in sluggish output response and increases cost. Though the average currents are low in these topologies, the capacitor peak currents are high, resulting in high current rated switches. Thereby, derates the device utilisation and also increases the cost. This paper proposes a new boost DC-link integrated multilevel inverter (BDIMLI), which overcomes the limitations of existing SCMLI topologies. Besides, the proposed inverter provides 9-, 11- and 13-level operations with less component count, reduced capacitor size, adjustable voltage gain. The experimental results and comparative analysis of proposed BDIMLI are presented.

The paper comprises of six sections. Section 2 presents the TBDC operating principle, inductor and capacitor design procedure. The proposed BDIMLI operation is clearly discussed in Section 3. A comprehensive comparison with existing MLI topologies is presented in Section 4. Section 5 presents experimental results for various load conditions and this paper is concluded in Section 6.

2 Two-level boost DC-link converter (TBDC)

Fig. 1 depicts the TBDC schematic, which comprises of two converters, namely conv-1 and conv-2. Conv-1 is a modified boost converter consisting of voltage source V_i, inductor L, boost switch S_b, diode D and capacitor C. Conv-2 is a level selector circuit comprising of two switches S_L and S_U, that makes the output voltage v_o across the load resistance R_o equal to either V_i (level-1) or $V_i + v_c$ (level-2), where v_c is the voltage across the capacitor C. Corresponding equivalent circuits of TBDC for level-1 and level-2 are shown in Figs. 2*a* and *b*, respectively. Fig. 2*c* illustrates the waveforms of TBDC, explaining its operation and control. Figs. 3*a* and *b* depict the typical output voltage waveform for conventional SCMLI basic cell and the TBDC unit, respectively. This clearly shows the drooping voltage during level-2 in the conventional SCMLI basic cell. The duration of level-2 decides the capacitor ripple voltage and its capacitance. Longer the duration, the larger will be the capacitor ripple or capacitance required. Operating modes of TBDC for level-1 and level-2 are explained as follows:

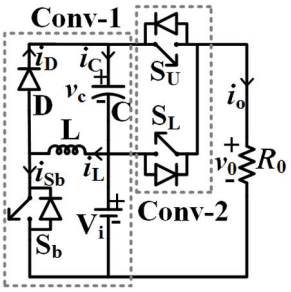

Fig. 1 *Two-level boost DC-link converter unit*

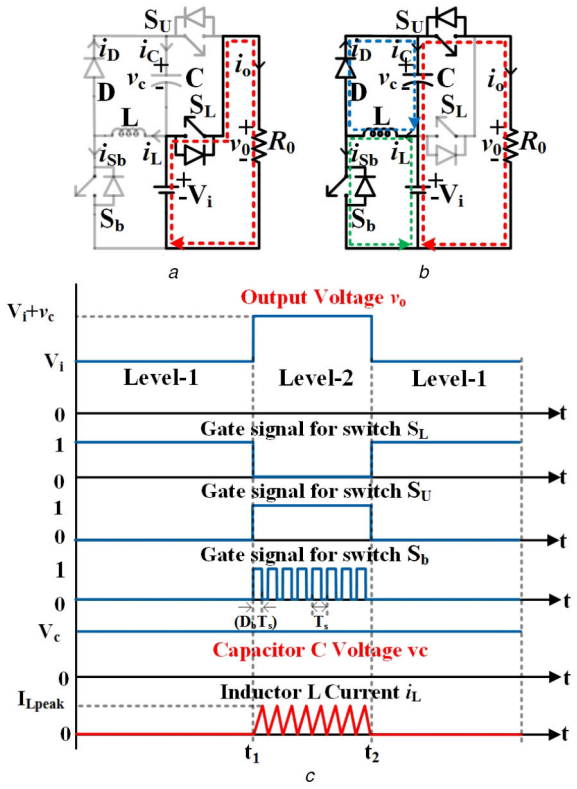

Fig. 2 *TBDC*

(a) Equivalent circuit for level-1, ***(b)*** Equivalent circuit for level-2, ***(c)*** Waveforms of the output voltage, switch gate pulses, capacitor voltage and inductor current during level-1 and level-2 operations

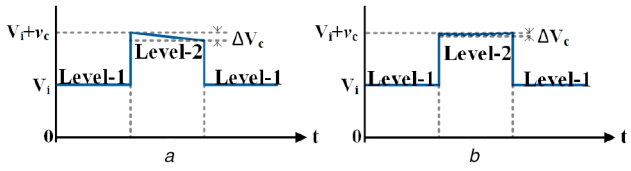

Fig. 3 *Typical output voltage waveform of*

(a) Conventional SCMLI basic cell, ***(b)*** TBDC unit

Level-1 ($0 \rightarrow t_1$ and $t > t_2$)*:* Fig. 2*a* depicts the equivalent circuit of level-1. During this interval, the switch S_L is turned ON while switches S_U and S_b are OFF. Thus, the load current conducts through the path $V_i - S_L - R_o - V_i$ and the voltage $v_o = V_i$.

Level-2 ($t_1 \rightarrow t_2$)*:* Fig. 2*b* depicts the equivalent circuit of level-2. During this interval, the switch S_U is ON and S_L is OFF continuously, while switch S_b operates with switching frequency f_s and duty cycle D_b to maintain desired capacitor voltage v_c. When S_b is ON, the diode D becomes reverse biased and inductor gets magnetised. During this period, the inductor current follows the dotted green line path, while the dotted blue line path is inactive. When S_b is OFF, the diode D becomes forward biased and the inductor current follows the dotted blue line path to charge the capacitor, while the dotted green line path is inactive. As S_U is continuously ON, thus the load current conducts through the path $V_i - v_c - S_U - R_o - V_i$. Hence, the input source and capacitor voltages are in series additive resulting in an output voltage $v_o = V_i + v_c$.

When S_b is ON: The inductor current increases linearly from 0 to its peak value I_{Lpeak} and conducts through the path $V_i - L - S_b - V_i$ as shown in Fig. 2*b*. The currents $i_{Sb} = i_L$, $i_D = 0$, $i_c = -i_o$, and the inductor peak current I_{Lpeak} is expressed as

$$v_L = L\frac{di_L}{dt} = V_i \tag{1}$$

$$I_{Lpeak} = \frac{V_i D_b}{L f_s} \tag{2}$$

where i_L, i_C, i_D, i_{Sb} and i_o are instantaneous currents through L, C, D_b, S_b and R_o, respectively, and v_L is the voltage across the inductor L.

When S_b is OFF: Diode D conducts and the stored inductor energy is used to charge the capacitor as well as to supply the load. Assume the capacitor voltage is constant (i.e. $v_c = V_c$). Here, the current $i_o = i_L - i_c$, $i_L = i_D$ and I_{Lpeak} is obtained as follows:

$$v_L = L\frac{di_L}{dt} = -V_c \tag{3}$$

$$I_{Lpeak} = \frac{V_c(1 - D_b)}{L f_s} \tag{4}$$

From (2) and (4)

$$V_c = \frac{D_b}{(1 - D_b)} V_i = nV_i \tag{5}$$

where n is the step-up ratio of the TBDC and expressed as

$$n = \frac{D_b}{(1 - D_b)}$$

2.1 Inductor design

At boundary conduction mode (BCM), the energy stored in the inductor should be completely transferred to the capacitor. The stored inductor energy in BCM is

$$E_L = \frac{1}{2} L_B I_{LBpeak}^2 \tag{6}$$

where L_B is critical inductance value and I_{LBpeak} is respective inductor peak current. The energy transferred to the capacitor is

$$E_c = V_c I_0 T_s \tag{7}$$

From (2), (6) and (7)

$$\frac{1}{2}L_{\mathrm{B}}I_{L_{\mathrm{B}}\mathrm{peak}}^{2} = V_{\mathrm{c}}I_{0}T_{\mathrm{s}} \tag{8}$$

$$L_{\mathrm{B}} = \frac{R_{0}D_{\mathrm{b}}^{2}}{2n(1+n)f_{\mathrm{s}}} \tag{9}$$

2.2 Capacitor design

The critical value of the capacitor can be determined as follows:

$$C_{\mathrm{cr}} = \frac{(V_{\mathrm{i}}+V_{\mathrm{c}})D}{R_{0}\Delta V_{\mathrm{c}}f_{\mathrm{s}}} = \frac{V_{\mathrm{c}}}{\Delta V_{\mathrm{c}}}\frac{(1+n)}{n}\frac{D}{R_{0}f_{\mathrm{s}}} \tag{10}$$

where ΔV_{c} is the capacitor voltage ripple and usually the capacitor value $C \geq C_{\mathrm{cr}}$.

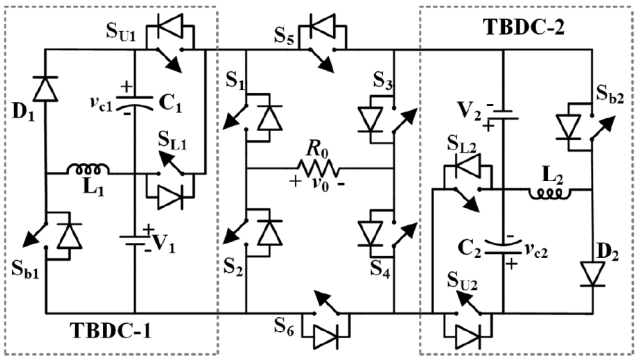

Fig. 4 *Schematic diagram of the proposed BDIMLI*

3 Design and operation of BDIMLI topology

The schematic diagram of the proposed BDIMLI is depicted in Fig. 4. It consists of two TBDC converters and one hybrid H-bridge formed by six switches ($S_1 - S_6$). The capacitors C_1 and C_2 are charged to the voltages V_{c1} and V_{c2}, respectively, where V_{c1} is n_1 times of V_1 and V_{c2} is n_2 times of V_2. The TBDC-1 output voltages are V_1 and $V_1 + V_{c1}$ for the respective conduction of S_{L1} and S_{U1}. Similarly, TBDC-2 output voltages are V_2 and $V_2 + V_{c2}$ for the respective conduction of S_{L2} and S_{U2}. Fig. 5 depicts the logical realisation of gate pulses for switches S_{b1} and S_{b2}, which are synchronised with gate pulses of S_{U1} and S_{U2}, respectively. D_{b1} and D_{b2} are the duty cycles of S_{b1} and S_{b2}, respectively. The BDIMLI achieves 9 or 11 or 13-level output voltage waveform by proper selection of V_{c1} and V_{c2}. Table 1 provides the respective capacitor voltages and step-up ratios (n_1 and n_2) for 9-, 11- and 13-level operations of BDIMLI. The switching states for 13-level operations are furnished in Table 2 respectively. The timing sequence and

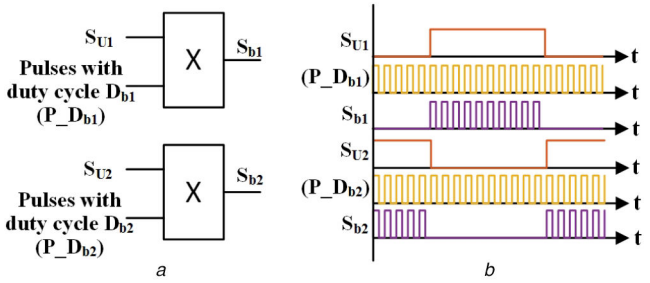

Fig. 5 *S_{b1} and S_{b2} gate pulses*
(a) Logic diagram, ***(b)*** Model waveforms

Table 1 Capacitor voltages, and step-up ratios for 9-, 11- and 13-level operations of BDIMLI

Level of operation	Voltage V_{c1}	Voltage V_{c2}	Step-up ratio n_1	Step-up ratio n_2
9-level	$1\,V_{\mathrm{dc}}$	$1\,V_{\mathrm{dc}}$	1	1
11-level	$1\,V_{\mathrm{dc}}$	$2\,V_{\mathrm{dc}}$	1	2
	$2\,V_{\mathrm{dc}}$	$1\,V_{\mathrm{dc}}$	2	1
13-level	$1\,V_{\mathrm{dc}}$	$3\,V_{\mathrm{dc}}$	1	3
	$3\,V_{\mathrm{dc}}$	$1\,V_{\mathrm{dc}}$	3	1

For all levels $V_1 = V_2 = V_{\mathrm{dc}}$.

Table 2 Switching states for 13-level output

On state switches	Boost converter		V_{o}	
	BC-1	BC-2		
S_2, S_4, S_6	OFF	OFF	0	
S_1, S_3, S_5				
S_{L1}, S_1, S_4, S_6	OFF	OFF	V_1	V_{dc}
S_{L2}, S_2, S_3, S_6			V_2	
S_{U1}, S_1, S_4, S_6	ON	OFF	$V_1 + V_{c1}$	$2V_{\mathrm{dc}}$
S_{L1}, S_{L2}, S_1, S_3, S_6	OFF	OFF	$V_1 + V_2$	
S_{U1}, S_{L2}, S_1, S_3, S_6	ON	OFF	$V_1 + V_2 + V_{c1}$	$3V_{\mathrm{dc}}$ [*t*]
S_{U2}, S_2, S_3, S_6	OFF	ON	$V_2 + V_{c2}$	$4V_{\mathrm{dc}}$ [*b*]
S_{L1}, S_{U2}, S_1, S_3, S_6	OFF	ON	$V_1 + V_2 + V_{c2}$	$5V_{\mathrm{dc}}$
S_{U1}, S_{U2}, S_1, S_3, S_6	ON	ON	$V_1 + V_2 + V_{c1} + V_{c2}$	$6V_{dc}$
S_{U1}, S_{U2}, S_2, S_4, S_5	ON	ON	$-(V_1 + V_2 + V_{c1} + V_{c2})$	$-6V_{\mathrm{dc}}$
S_{L1}, S_{U2}, S_2, S_4, S_5	OFF	ON	$-(V_1 + V_2 + V_{c2})$	$-5V_{\mathrm{dc}}$
S_{U2}, S_1, S_4, S_5	OFF	ON	$-(V_2 + V_{c2})$	$-4V_{\mathrm{dc}}$
S_{U1}, S_{L2}, S_2, S_4, S_5	ON	OFF	$-(V_1 + V_2 + V_{c1})$	$-3V_{\mathrm{dc}}$
S_{U1}, S_2, S_3, S_5	ON	OFF	$-(V_1 + V_{c1})$	$-2V_{\mathrm{dc}}$
S_{L1}, S_{L2}, S_2, S_4, S_5	OFF	OFF	$-(V_1 + V_2)$	
S_{L1}, S_2, S_3, S_5	OFF	OFF	$-(V_1)$	$-1V_{\mathrm{dc}}$
S_{L2}, S_1, S_4, S_5			$-(V_2)$	

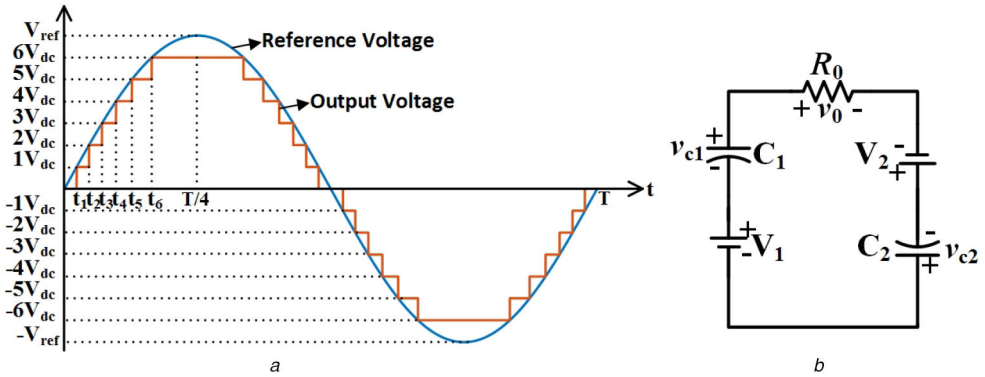

Fig. 6 *BDIMLI switching modulation logic and design*

(a) Model waveform of the 13-level output voltage, ***(b)*** Equivalent circuit of BDIMLI for peak output voltage

corresponding switching states for each level of the 13-level output voltage are realised from Fig. 6*a* and Table 2.

Similarly, the timing sequence and switching states for each level of 9- and 11-level output voltages can be realised. Fig. 7 illustrates the equivalent circuits for each level of 13-level BDIMLI operation. The generalised output voltage of BDIMLI is given by

$$v_{\mathrm{o}} = v_{o1}[(S_3 + S_4)(S_1S_6 - S_2S_5)] + v_{o2}[(S_1 + S_2)(S_3S_6 - S_4S_5)] \tag{11}$$

where

$$v_{o1} = [S_{L1} + (1 + n_1)S_{U1}]V_1$$

$$v_{o2} = [S_{L2} + (1 + n_2)S_{U2}]V_2$$

The TBDC-1 and TBDC-2 topologies are designed to operate in BCM mode and their respective critical inductor values L_{B1} and L_{B2} of L_1 and L_2 are obtained by considering the highest output voltage level. From Fig. 6*b*, the peak value of output current is given by

$$i_{\mathrm{o,max}} = \frac{V_1 + V_2 + V_{c1} + V_{c2}}{R_{\mathrm{o}}} = \frac{(2 + n_1 + n_2)V_{\mathrm{dc}}}{R_{\mathrm{o}}} \tag{12}$$

Maximum powers P_{c1} and P_{c2} delivered by capacitors C_1 and C_2 are given by

$$P_{c1} = V_{c1}\, i_{\mathrm{o,max}} = \frac{n_1(2 + n_1 + n_2)V_{\mathrm{dc}}^2}{R_{\mathrm{o}}} \tag{13}$$

$$P_{c2} = V_{c2}\, i_{\mathrm{o,max}} = \frac{n_2(2 + n_1 + n_2)V_{\mathrm{dc}}^2}{R_{\mathrm{o}}} \tag{14}$$

From (8), (9), (13) and (14), the critical values of L_{B1} and L_{B2} are expressed as follows:

$$L_{B1} = \frac{R_{\mathrm{o}}D_{b1}^2}{2n_1(2 + n_1 + n_2)f_{\mathrm{s}}} \tag{15}$$

$$L_{B2} = \frac{R_{\mathrm{o}}D_{b2}^2}{2n_2(2 + n_1 + n_2)f_{\mathrm{s}}} \tag{16}$$

From (15) and (16), the characteristics of L_{B1} and L_{B2} as a function of R_{o} for 9-level and 13-level operations with f_{s} of 10, 30 and 50 kHz are illustrated in Figs. 8*a* and 9*a*, respectively. For DCM operation, inductors L_1 and L_2 should be less than the L_{B1} and L_{B2}, respectively, and should be higher for CCM operation. It can be noticed from Figs. 8*a* and 9*a* that for a particular power rating, the inductor size decreases with an increase in the switching frequency. From (10), (15) and (16), the minimum capacitances $C_{1\,\mathrm{min}}$ and $C_{2\,\mathrm{min}}$ of C_1 and C_2 required to limit ripple voltage to ΔV_{c1} and ΔV_{c2}, respectively, are given as follows:

$$C_{1\,\mathrm{min}} = \frac{V_{c1}(2 + n_1 + n_2)D_{b1}}{\Delta V_{c1}n_1R_0f_{\mathrm{s}}} = \frac{(2 + n_1 + n_2)D_{b1}}{x_1n_1R_0f_{\mathrm{s}}} \tag{17}$$

$$C_{2\,\mathrm{min}} = \frac{V_{c2}(2 + n_1 + n_2)D_{b2}}{\Delta V_{c2}n_2R_0f_{\mathrm{s}}} = \frac{(2 + n_1 + n_2)D_{b2}}{x_2n_2R_0f_{\mathrm{s}}} \tag{18}$$

where x_1 and x_2 are the ratios of corresponding capacitor ripple voltage to average capacitor voltage of C_1 and C_2, respectively, or

$$C_{1\,\mathrm{min}} = \frac{P_{\mathrm{max}}D_{b1}}{x_1n_1(2 + n_1 + n_2)f_{\mathrm{s}}V_1^2} \tag{19}$$

$$C_{2\,\mathrm{min}} = \frac{P_{\mathrm{max}}D_{b2}}{x_2n_2(2 + n_1 + n_2)f_{\mathrm{s}}V_1^2} \tag{20}$$

where P_{max} is the maximum power of the BDIMLI and expressed as

$$P_{\mathrm{max}} = \frac{(2 + n_1 + n_2)V_1^2}{R_{\mathrm{o}}}$$

Both capacitors C_1 and C_2 are charged at a high switching frequency while feeding the load is fed at power frequency. Hence, small size capacitors are adequate even at high power ratings. From (17)–(20), the characteristics of $C_{1\,\mathrm{min}}$ and $C_{2\,\mathrm{min}}$ as a function of R_{o} and P_{o} with $f_{\mathrm{s}} = 10$ kHz for 9-level and l3-level operations are illustrated in Figs. 8*b*, *c* and 9*b*, *c*, respectively. From the characteristics of $C_{1\,\mathrm{min}}$ and $C_{2\,\mathrm{min}}$, the minimum capacitor value for a specific power rating can be identified.

4 Comparison with existing topologies

The comparative analysis of proposed BDIMLI with different existing MLI topologies in terms of component count, capacitor size, total switch voltage (TSV), cost and boost factor is presented as follows.

4.1 Component count and boost-factor

Various key parameters of proposed BDIMLI and existing SCMLI topologies are compared at symmetric voltage sources. All the topologies are analysed for an output power (P_{o}) of 1000 W at $f_{\mathrm{o}} = 50$ Hz. The switching frequency of boost converters used in the proposed BDIMLI is 10 kHz. The capacitor values in each topology are calculated by assuming 5% capacitor voltage ripple and are presented in Tables 3 and 4 for 9- and 13-level outputs. The boost factor used for the comparison is expressed as

$$\text{Boost factor} = \frac{\text{Peak output voltage}(V_{\mathrm{o,peak}})}{\text{Sum of source voltages}(V_1 + V_2 + \cdots + V_n)} \tag{21}$$

4.1.1 For 9-level: From Table 3, it can be observed that the boost factor of BDIMLI is the same as existing 9-level SCMLI

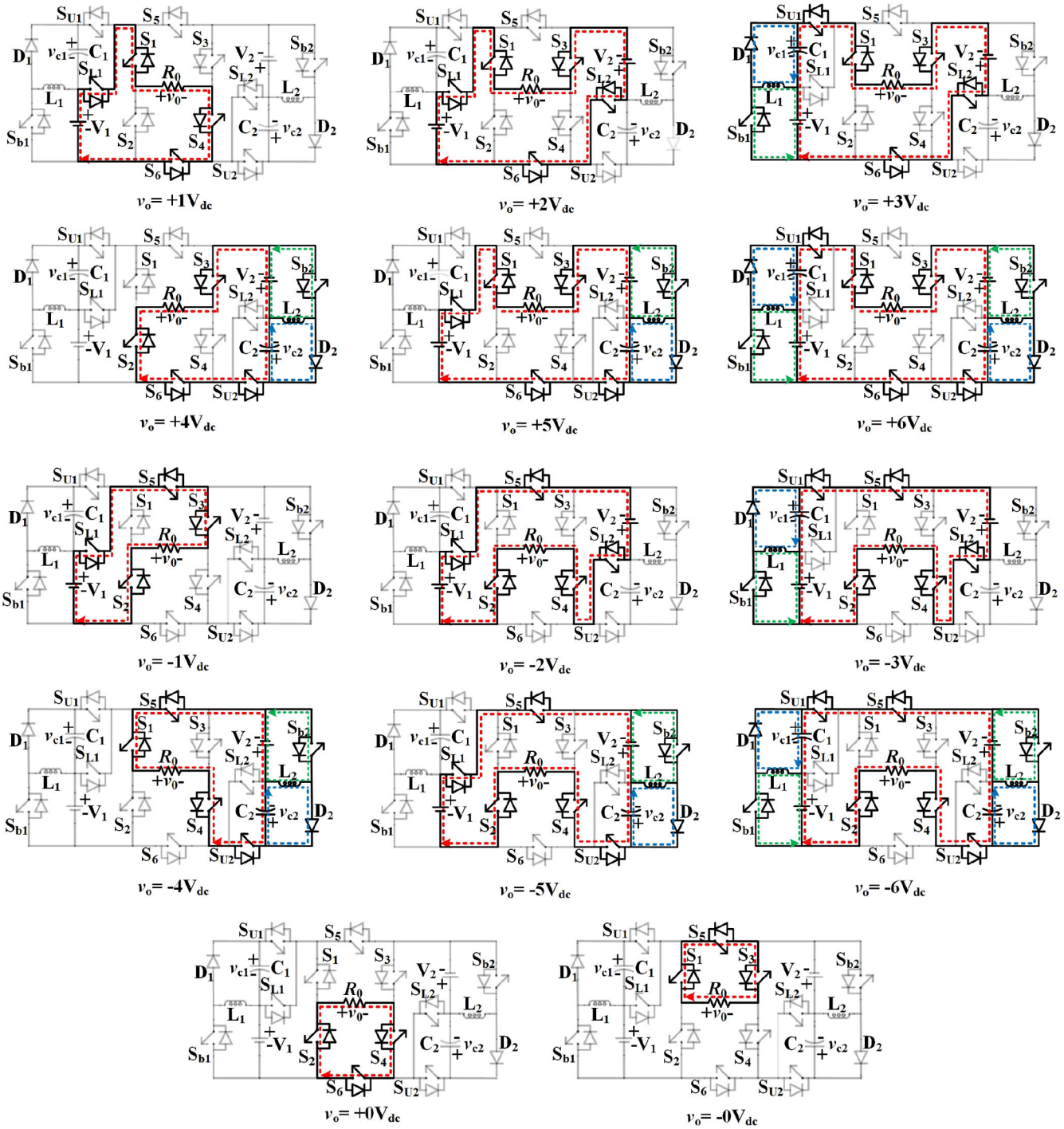

Fig. 7 *Different modes of operation of the proposed BDIMLI for 13-level operation*

topologies presented in [16, 18]. The size of the capacitors used for proposed BDIMLI is reduced by ~60–100 times as compared with the other SCMLI counterparts. Topology presented in [9] requires less number of switches, but requires more number of sources and also lack of boosting capability.

4.1.2 For 13-level: From Table 4, it can be noticed that the proposed BDIMLI with high boost factor has reduced the count of switches as well as capacitors when compared with the other topologies presented. In this case, the capacitor size is reduced by ~100 times in comparison with the other MLIs.

Even though the proposed BDIMLI utilises inductors, these are in terms of micro Henrys. Thus, it occupies less space and highly economical compared to the MLIs with bulky electrolytic capacitors.

Further, the voltage and current stresses of the various switches presented in the BDIMLI and the other step-up MLIs are provided in Table 5. The nearest rated components are considered for the cost comparison, which is also presented in Table 5. From this table, it can be observed that the cost of the capacitors used in the proposed topology is very less. Even though the BDIMLI utilises additional components like voltage sensors and inductors, the overall cost is relatively lesser than the other step-up MLIs presented in Table 5.

4.2 Efficiency

To examine the efficient operation of BDIMLI, various power losses and overall efficiency for different output power ratings are evaluated. The expressions given in [4, 16] are employed to calculate power losses (switching and conduction losses of semiconductor devices, and conduction losses of passive components). The thermal model of the BDIMLI is simulated for 9- and 13-level operations as explained in [19] using PSIM to evaluate various power losses and the results are presented in

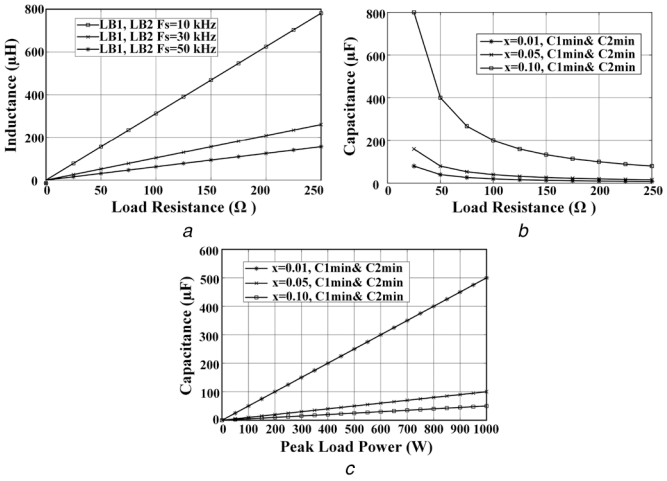

Fig. 8 *Design characteristics for 9-level operation*

(a) L_{B1} and L_{B2} versus R_o at $f_s = 10,\ 30$ and 50 kHz, ***(b)*** $C_{1\,min}$ and $C_{2\,min}$ versus R_o at $f_s = 10$ kHz for different ripple voltages, ***(c)*** $C_{1\,min}$ and $C_{2\,min}$ versus P_{max} at $f_s = 10$kHz and $V_1 = 50$ V

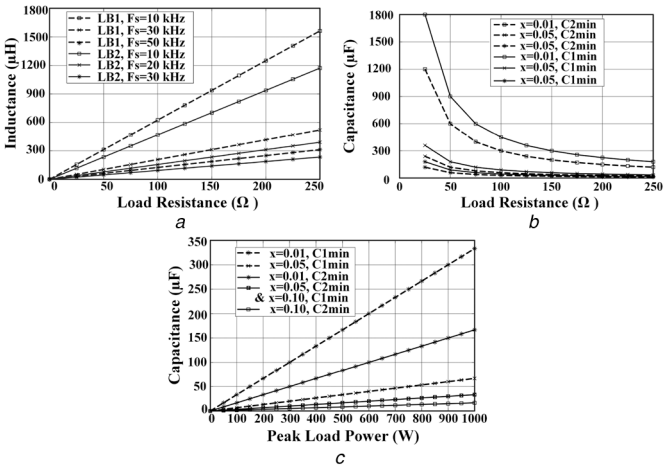

Fig. 9 *Design characteristics for 13-level operation*

(a) L_{B1} and L_{B2} versus R_o at $f_s = 10,\ 30$ and50 kHz, ***(b)*** $C_{1\,min}$ and $C_{2\,min}$ versus R_o at $f_s = 10$ kHz for different ripple voltages, ***(c)*** $C_{1\,min}$ and $C_{2\,min}$ versus P_{max} with $f_s = 10$ kHz and $V_1 = 50$ V

Table 3 Comparison of proposed BDIMLI with existing MLI topologies at the symmetric condition of the involved DC source for 9-level output ($P_o = 1000$ W, $V_{o,peak} = 200$ V and $f_o = 50$ Hz)

Topology	*N_sources*	*N_switches*	*N_diodes*	*N_capacitors*	Capacitors values	*N_inductors*	TSV	$\frac{TSV}{V_{o,peak}}$	Boost factor
[9]	4	10	—	—	—	—	1000	5	1
[16]-(1)	2	12	2	2	*C*1 = 21.5 mF				
					*C*2 = 21.5 mF	—	1000	5	2
[18]-(1)	2	12	0	1	*C*1 = 13.6 mF	—	1100	5.5	2
proposed (with $f_s = 10$ kHz	2	12	2	2	*C*1 = 0.2 mF	2	1400	7	2
$L_1 = L_2 = 62.5\ \mu$H)					*C*2 = 0.2 mF				

Table 4 Comparison of proposed BDIMLI with existing MLI topologies at the symmetric condition of the involved DC source for 13-level output ($P_o = 1000$ W, $V_{o,peak} = 300$ V and $f_o = 50$ Hz)

Topology	*N_sources*	*N_switches*	*N_diodes*	*N_capacitors*	Capacitors values	*N_inductors*	TSV	$\frac{TSV}{V_{o,peak}}$	Boost factor
[16]-(1) and -(1)	3	18	3	3	*C*1 = *C*3 = 15 mF	—	1500	5	2
					*C*2 = 13 mF				
[16]-(2)	2	14	4	4	*C*1 = *C*2 = 17.5 mF	—	1600	5.33	3
					*C*1P = *C*2P = 13.5 mF				
[18]-(2)	2	18	—	2	*C*1 = *C*2 = 15 mF	—	1650	3	
proposed (with $f_s = 10$ kHz	2	12	2	2	*C*1 = 0.12 mF	2	1900	6.33	3
$L_1 = 104\ \mu$H, $L_2 = 78\ \mu$H)					*C*2 = 0.06 mF				

Table 6 and the corresponding efficiency curves are shown in Fig. 10. From these, it is evident that the efficiency of BDIMLI increases with an increase in output power. Whereas the existing MLI [16] topologies provide peak efficiency at low power, but droops with the increase in power rating.

5 Experimental results

An experimental prototype of the proposed BDIMLI is developed and illustrated in Fig. 11. Gating pulses for all the switching devices of BDIMLI are realised with the TMS320F28379d processor. S_{b1} and S_{b2} are operated with 10 kHz switching frequency and S_5 and S_6 are operated with a power frequency of 50 Hz. While the rest of the switches are operated with low frequencies (i.e. approximately five to six times of the fundamental frequency) depending on the switching states. To regulate the capacitor voltages to the desired values, two PI controllers are employed. Figs. 12*a* and *b* illustrate the experimental waveforms of load, inductors, capacitors and input voltage sources for 9-level (540 W) and 13-level (580 W) operations, respectively. The tested experimental prototype provides 85.7 and 83.2% for 13- and 9-level operations with R-load as per the specifications in Table 7.

Table 5 Cost comparison of the proposed BDIMLI with other step-up MLI topologies for 13-level operation at $P_o = 1000$ W

Topology	Component	Required rating	Component no	Quantity	Unit price, $	Amount, $
[16]-(1)	S1a-S1d, S2a-S2d	150 V/7 A	IRLS640A	8	1.49	11.92
	S1, S2	100 V/35 A	IRFB41N15DPBF	2	2.21	4.42
	S11, S111, S22, S222	50 V/17 A	FDPF3860T	4	1.07	4.28
	D1, D2	100 V/35 A	VF40150C-M3/4W	2	1.64	3.28
	D11, D111, D22, D222	50 V/7 A	RB088T100HZC9	4	0.84	3.36
	C11, C22	17.5 mF/50 V	36DY183F075BC2A	2	59.71	119.42
	C1, C2	13.5 mF/50 V	DCM143U075BE2B	2	35.34	70.68
	drivers		A3120 with auxiliaries	14	10	140
	voltage sensors					not used
					total cost ($)	357.36
[16]-(2)	S1a-S1d, S2a-S2d, S3a-S3d	100 V/7 A	FDPF770N15A	12	1.37	16.44
	S1, S2, S3	50 V/27 A	STF45N10F7	3	2.16	6.48
	S11, S22, S33	50 V/7 A	FQU13N10LTU	3	0.75	2.25
	D1, D2, D3	50 V/27 A	DST30100C	3	1.41	4.23
	C1, C2, C3	15 mF,50 V	CGS153U075V5L	3	41.77	125.31
	drivers		A3120 with auxiliaries	18	10	180
	voltage sensors					not used
					Total cost ($)	334.71
[18]	S1, S3a, S3b, S5, S7, S8a, S8b	100 V,/26 A	FDP2572	7	1.82	12.74
	S2, S4, S6, S9–14	100 V/7 A	FDPF770N15A	9	1.37	12.33
	ST1a, ST1b	50 V/7 A	FQU13N10LTU	2	0.75	1.5
	C1,C2	11 mF/100 V	DCMX113U150CC2B	2	61.82	123.64
	drivers		A3120 with auxiliaries	18	10	180
	voltage sensors					not used
					total cost, $	330.21
proposed	S1, S2	100 V/7 A	FDPF770N15A	2	1.37	2.74
	S3, S4	200 V/7 A	RCX100N25	2	1.86	3.72
	S5, S6	300 V/7 A	IRF740PBF	2	1.53	3.06
	SL1, SU1	50 V/6 A	FQU13N10LTU	2	0.75	1.5
	SL2, SU2	150 V/6 A	IRLS640A	2	1.49	2.98
	SB1	100 V/22 A	SQP25N15-52GE3	1	1.95	1.95
	SB2	200 V/44 A	IRF300P227	1	5.94	5.94
	DB1	100 V/22 A	TST30H150CW C0G	1	1.58	1.58
	Db2	200 V/44 A	SBR60A300CT	1	3.92	3.92
	C1	120 μF/50 V	672D127H075ET5C	1	5.06	5.06
	C2	60 μF/150 V	WBR60-250A	1	10.73	10.73
	L1	104 μH/38 A	B66387G1000X187	1	10	10
	L2	78 μH/38 A	B66387G1000X188	1	10	10
	drivers		A3120 with auxiliaries	12	10	120
	voltage sensors		LEM-LV25P	2	65	130
					total cost, $	313.18

Note: Nearest available rated components are selected.

Table 6 Loss analysis of the proposed BDIMLI for 9- and 13-level operations using PSIM

Mode of operation	$P_o = 200$ W			$P_o = 400$ W			$P_o = 600$ W			$P_o = 800$ W			$P_o = 1000$ W		
	P_{swi}	P_{cond}	P_{lc}^*	P_{swi}	P_{cond}	P_{lc}^*	P_{swi}	P_{cond}	P_{lc}^*	P_{swi}	P_{cond}	P_{lc}^*	P_{swi}	P_{cond}	P_{lc}^*
(9-level)	0.3006	20.4	2.0908	0.548	30.35	4.0914	0.7801	38.98	6.2149	1.037	46.67	8.2922	1.317	53.85	10.632
(13-level)	0.5206	14.71	2.6012	1.02	24.21	5.194	1.527	32.7	9.282	1.937	39.16	10.237	2.478	46.87	12.851

Where P_{swi} = total switching losses, P_{cond} = total conduction losses, and P_{lc}^* = total passive component power losses.

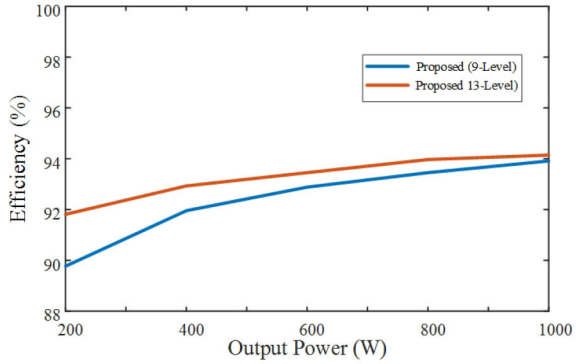

Fig. 10 *Efficiency curves of proposed BDIMLI*

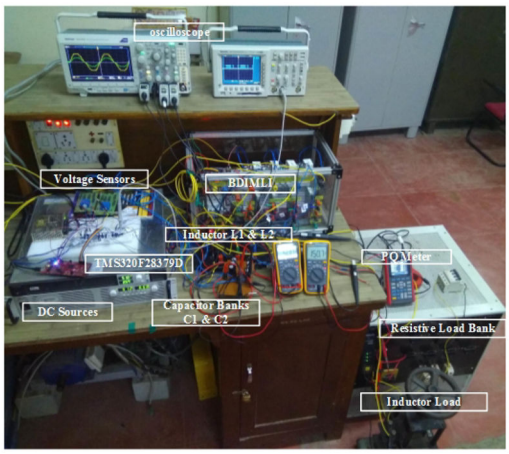

Fig. 11 *Experimental prototype of proposed BDIMLI*

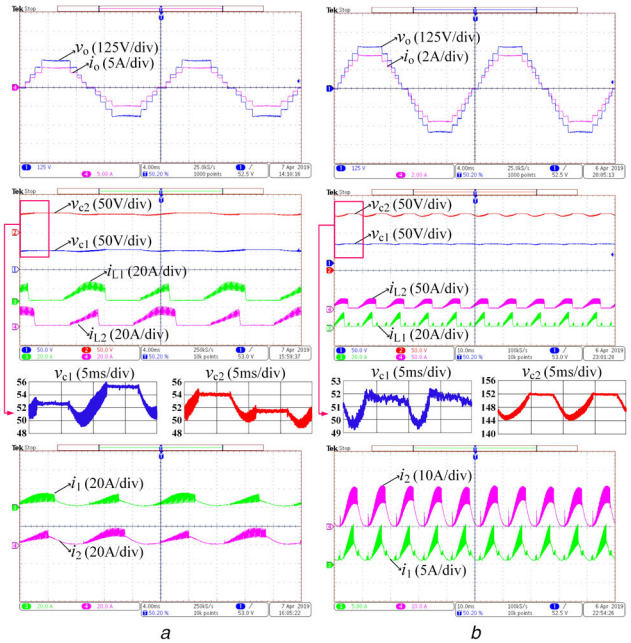

Fig. 12 *Experimental waveforms of load voltage v_o, load current i_o, inductors L_1, L_2 currents (i_{L1}, i_{L2}) capacitors C_1, C_2 voltages (v_{c1} and v_{c2}) and dc voltage source currents(i_1 and i_2) for*
(a) 9-level operation, ***(b)*** 13-level operation

Figs. 13*a* and *b* present the blocking voltage of switches (S_2, S_4, S_5, S_6, S_{L1}, S_{L2}, S_{b1} and S_{b2}) for 13-level operation.

The negative terminal of the voltage source V_2 is taken as a reference to measure the CMV of BDIMLI and the experimental CMV waveform is shown in Fig. 14*a*. To measure the source leakage currents (i_{lg1} and i_{lg2}), a series combination of parasitic capacitance $C_p = 100\,\text{nF}$ and parasitic resistance ($R_p = 10\,\Omega$) is

Table 7 Specification and design parameters of BDIMLI

Parameter	Value/part number
$V_1 = V_2$	50 V
f_o	50 Hz
f_s	10 kHz
V_o(RMS)	220 V (13-level), 150 V (9-level)
P_o	580 W (13-level), 540 W (9-level)
R_o	80 Ω (13-level), 40 Ω (9-level)
L_1, L_2	500, 500 µH
C_1, C_2	200 µF/400 V, 200 µF/400 V
switches	IKW40T120
diodes	STPSC2006CW

connected from each source positive terminal to load negative terminal. From Fig. 14*b*, it can be observed that the measured i_{lg1} and i_{lg2} RMS values are 5.649 and 6.066 mA, which are compatible with the VDE0126-1-1 standard. The dynamic behaviour of the proposed BDIMLI is depicted in Figs. 15*a* and *b* for different load changing conditions confirming a smooth and stable operation. During the transition from no-load to full-load, it can be observed that there is a dip in load voltage. However, the PI controllers employed to track the load voltage to its nominal value. From this figure, it is also evident that there is no deviation in load voltage during the change in load type (i.e. *R* to *R–L* and vice-versa). Single-phase power quality analyser (PQA) UT-283A is used to measure the total harmonic distortion (THD). Figs. 16*a* and *b* present the harmonic spectrum of load voltage for both operating levels. As the proposed BDIMLI utilises the fundamental switching frequency, the dominant harmonic will be at lower order. The PQA used can measure up to the 50th order harmonic component for the THD calculation. The measured THD of the load voltage without any filter is obtained as 10.1 and 6.69% for 9-level and 13-level operations, respectively. From these THD results, it can be noticed

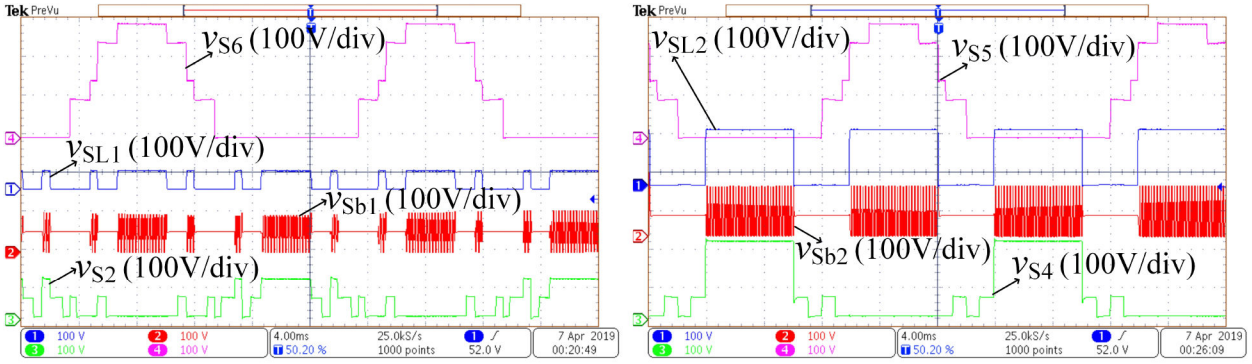

Fig. 13 *Experimental waveforms of 13-level operation*
(a) PIV of S_2, S_6, S_{L1}, S_{b1}, ***(b)*** PIV of S_4, S_5, S_{L2}, S_{b2}

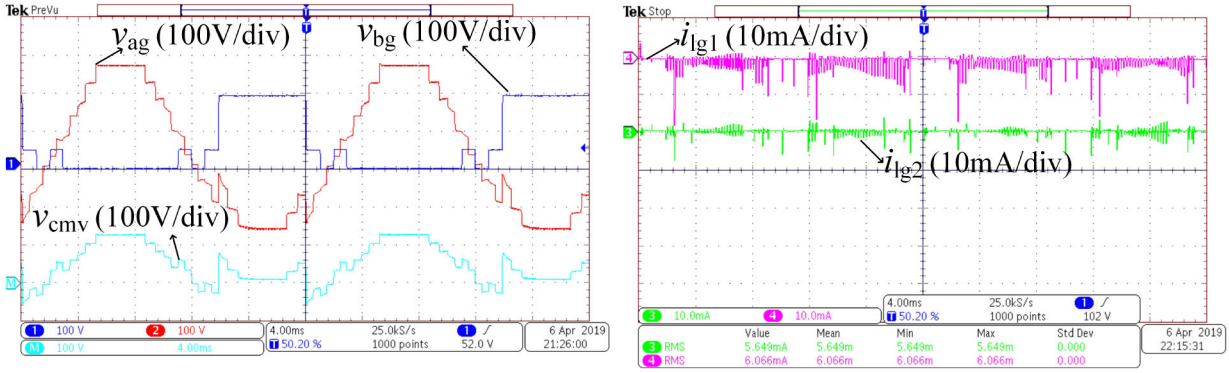

Fig. 14 *Experimental waveforms of 13-level operation*
(a) CMV, ***(b)*** DC source leakage currents i_{lg1} and i_{lg2}

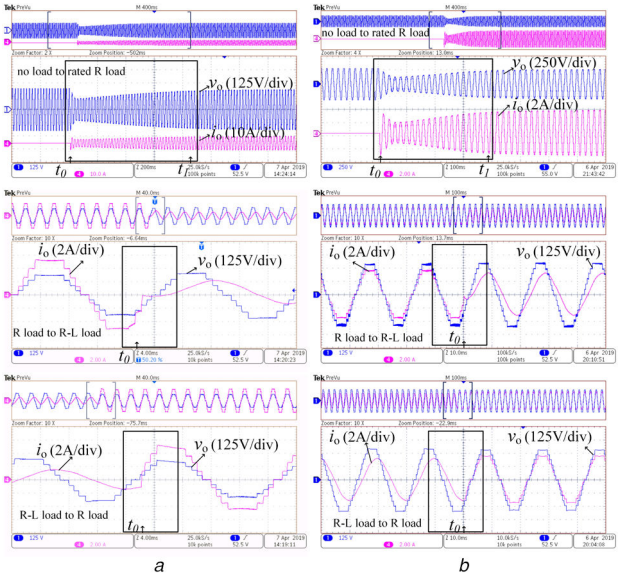

Fig. 15 *Dynamic behaviour of the proposed BDIMLI with step change in load conditions: no-load to rated R load, R load to R–L load, and R–L load to R load for*
(a) 9-level operation, ***(b)*** 13-level operation

that the fifth-order harmonic is dominant in the output voltage than the third order, thus requires a small filter. A comparison of experimental %THD of the BDIMLI and the MLI proposed in [16] is presented in Table 8, which shows the %THD is less in the proposed BDIMLI.

6 Conclusion

In this paper, a novel boost DC-link integrated multilevel inverter is proposed. The proposed BDIMLI provides various advantages such as high boost-factor, reduced capacitor size, relatively low cost, with low THD and component count. The design characteristics of inductors and capacitors are analysed, which shows a significant reduction in capacitor size. In addition, the capacitor voltages are constant irrespective of load changing conditions for 9-level and 13-level operations. The benefits of proposed BDIMLI are justified with the comparative study in contrast to recent MLI topologies. Moreover, the dynamic behaviour of BDIMLI under various load conditions is tested with

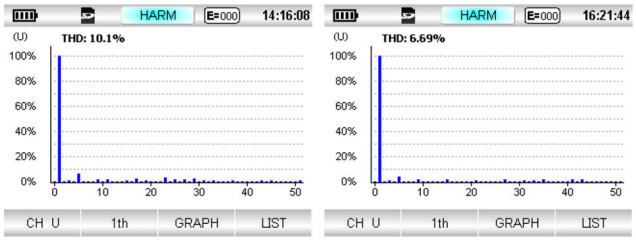

Fig. 16 *Harmonic spectrum of load voltage v_o for*
(a) 9-level operation, ***(b)*** 13-level operation

Table 8 Comparison of experimental THD of the proposed BDIMLI with the MLI presented in [16]

Parameter	Proposed BDIMLI	Cascaded MLI [16]
modulation	nearest level control	phase shift modulation
THD (9-level)	10.1%	19.1%
THD (13-level)	6.69%	14.1%

no-load, resistive and inductive loads providing a smooth and stable operation.

7 Acknowledgement

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